REMARKS

This application has been carefully reviewed in light of the Office Action dated June 4, 2008. Claims 1, 3 to 7, 20, 22 to 26 and 39 remain in the application, of which Claims 1, 20 and 39 are independent. Reconsideration and further examination are respectfully requested.

Claims 1, 3, 7, 20, 22, 26 and 39 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,488,673 (Katayama), and Claims 4 to 6 and 23 to 25 were rejected under § 103(a) over Katayama further in view of U.S. Patent No. 6,977,756 (Nakano). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention reduces the necessary memory for processing image data since the quantization component quantizes only the integral portion (upper bits) of corrected image data without quantizing the decimal portion (lower bits) of the corrected image data, and the buffer stores a calculated quantization error that is to be diffused to the next pixel.

Referring specifically to the claims, amended independent Claim 1 is directed to an image processing apparatus comprising a bit connection component that connects a decimal portion of image data of a preceding pixel to image data of a target pixel as lower bits of the image data of the target pixel, a correction component that generates corrected image data by adding a correction value to the bit-connected image data of the target pixel, a latch component that latches a decimal portion of the corrected image data to be connected to image data of a next pixel, a quantization component that quantizes an integral portion (upper bits) of the corrected image data without quantizing the decimal portion (lower bits) of the corrected image data, a calculation component that

calculates a quantization error, which is generated by quantization of the integral portion of the corrected image data by said quantization component, a buffer that stores the calculated quantization error for the integral portion of the corrected image data; and an error diffusion component that generates a correction value to be added to input data of a next pixel by diffusing the quantization error stored in said buffer.

Claims 20 and 39 are method and computer medium claims, respectively, that substantially correspond to Claim 1.

The applied art, alone or in any permissible combination, is not seen to disclose or to suggest the features of Claims 1, 20 and 39, and in particular, is not seen to disclose or to suggest at least the features of a quantization component (step) that quantizes an integral portion (upper bits) of the corrected image data without quantizing the decimal portion (lower bits) of the corrected image data, a calculation component (step) that calculates a quantization error, which is generated by quantization of the integral portion of the corrected image data, and a diffusion component (step) that generates a correction value to be added to input data of a next pixel by diffusing the quantization error which is stored in a buffer.

Katayama relates to the compensation of arithmetic error generated by error diffusion, whereby error data is added to pixel data of an objective pixel. The sum of the error data and the pixel data of the objective pixel are binarized, and a distribution error is calculated, which is generated in the binarization, and distributed to appropriate neighboring pixels. Finally, the total sum of the truncated decimal portions is distributed to neighboring pixels. However, the quantization part of Kayayama is not a component that only quantizes the integral portion (upper bits) of the corrected image data without

quantizing the decimal portion (lower bits) of the corrected image data. Therefore, Katayama cannot provide the benefit of reducing the buffer as in the present invention. Accordingly, Claims 1, 20 and 39 are believed to be allowable over Katayama.

Nakano is not seen to make up for the deficiencies of Katayama. In this regard, Nakano discloses that a data driven type processing device has an error diffusion computing unit built therein. An error holding register is provided within the error diffusion-computing unit, and is used to successively store and update a value of error information of a pixel that is to be diffused to a neighboring pixel being processed continuously. An error data memory is provided outside the computing unit, and is used to store and update a value of the error information that is to be diffused to another neighboring pixel being processed discontinuously. The error information and the values to be diffused are stored in a packet, and the packet is circulated for operation. However, Nakano is not seen to disclose or to suggest anything that, when combined with Katayama, would have resulted in at least the features of a quantization component (step) that quantizes an integral portion (upper bits) of the corrected image data without quantizing the decimal portion (lower bits) of the corrected image data, a calculation component (step) that calculates a quantization error, which is generated by quantization of the integral portion of the corrected image data, and a diffusion component (step) that generates a correction value to be added to input data of a next pixel by diffusing the quantization error which is stored in a buffer.

Thus, Claims 1, 20 and 39, as well as the claims dependent therefrom, are believed to be allowable.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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